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TIMELINEZ

VOLUME 7 ISSUE 05,06 MAY/JUNE 1989 $1.50

TIMEX/sinclair User Group News-Magazine

VIEW FROM RAMTOP

TIMELINEZ IS NOW SIX!
HAPPY BIRTHDAY TIMELINEZ.

This months column will be brief. We received in the mail what we felt is important information concerning the expandability of the TIMEXsinclair 2068. If any questions result from your reading, please consult your inquiries to:

Mr. William J. Pedersen
1120 Merrifield S.E.
Grand Rapids, MI 49507
The WIDJUP Co.

Please excuse the size of text used. This article is extreemly large.

On another note: Starting in August, the TIMEXsinclair Cambridge Silicon Valley Users (phew! a lot of words) will have their meeting on the third Wednesday of each month. Also, there are two more BBS's within our area. Let's show our support and give them a call!

The TIMEXsinclair 2068
By William J. Petersen

Dear Survivor,

The enclosed article regarding expanded bank switching is of such importance that I am sending it to several news letters to avoid delay with exchanges.

It is high time that memory and back-plane expansions become available and known.

The WIDJUP Co. is thereby making the original design public in the hope that it will get the ball rolling.

In the interest of economy and availability, two items should be accepted as an interim standard.

REMINDER
The July/August TIMELINEZ is a bi-monthly issue to maintain a 10/year subscription balance

The TIMEXsinclair 2068 Cont.

1. Back-Plane EVEREX SYSTEMS INC. EV-1085
2. Adapter WIDJUP Co. (Design)

This back-plane is a standard PC expansion board having eight slots; one of which must be used for the BSC. There is no need to make things difficult.

The adapter plugs into the rear connector and has the usual feed-thru. It has a cable take-off for connection to the BSC card, and some other convenience features. Design information will be available from the WIDJUP Co. It is hoped that someone will produce it. Prototypes have been made and examined at conventions for a couple of years, so this item should be nothing new.

There is one more thing that should be standardized, though the reasoning for it is not immediately evident. The pin assignments for the back-plane, being arbitrary anyway, will correspond closely with the IBM bus. The reason?

The BSC can easily be modified for use with some PC clone cards. Why not have upward compatibility right from the start. This is NOT a plug for IBM or the PC clones! It is a simple economy measure which is in the interest of all TS2068 supporters. There is no easier way to get ports, timers, and modems than this.

It will be a long time before users will be ready for a full-fledged auto-configuring system with a DAISY CHAIN, and the advanced BSC that requires, if ever. Hopefully a clone will come along having this built in. If anyone is doing that, I beg him to contact me. It EXISTS, regardless of what people have been saying. (It requires the EVEREX expansion board for the AT or eqivalent.)

Don't let this revolutionary development get away!

MEMORY IMPROVES WITH AGE ?

Crazy? Perhaps so, but survival of our favorite antique TS2068 computer depends on it to a degree. Two advances are primarily responsible for this. Both extend the amount and speed of available memory, over and beyond that in the DOCK bank.

Disc drives improve speed, accessibility and convenience over tape recording.

RAMDISK has broken all speed records and has expansion possibilities which are impressive.

Now all we need to do is find some way to bank switch additional memory. It has been said it can't be done because TIMEX expertise has been dispersed -- DINOSAUR CHIPS !

While it is true that the system TIMEX intended (before killing it) is highly complex, it is NOT the only system which works. The one described in Figures 1 and 2 is just about the minimum bank switching system. There are a lot of features like handling interrupts and autoconfiguring that are beyond it, but it can address 16 megabytes of memory and works with the unmodified TS2068.

TIMELINEZ

TIMEXsinclair user group News-Magazine

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1000, 1500, 2068

Sinclair's
ZX Spectrum+ 128K
Quantum Leap (QL)

Cambridge's Z88

FRONT PAGE

PRINTED USING sinclair QL PROFESSIONAL COMPUTER AND THIS PROGRAM.

DESK-TOP PUBLISHING
FOR THE SINCLAIR QL

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Issues 1/88 - present, contact your editor at **American Micro.**

The PDSE Library is now available to all; covering T/S1000-1500, T/S 2068, Spectrum and the QL.
Contact **American Micro** for further details.

The TIMEXsinclair 2068 Cont.

MEMORY BANK (Figure 2)

There is nothing particularly special about this memory bank. It decodes a 24 bit address and has a dip-switch to locate 64K of contiguous memory space at any 64K boundary.

If any of it's memory is active, it drives the BE signal low to disable LOCAL HOME, EXROM and DOCK banks. With this system it is impossible for two expansion banks to be on the bus at the same instant. (See Appendix A for greater detail.)

SYSTEM CONFIGURATION

There must be some way to MAP all or part of memory.

The simplest way to do this is to write programs which assume continuous memory up to a variable limit, and warn you when that limit is exceeded. For this, each expansion bank should have dip switches set from 1 to MAXBANK in sequence.

There are better ways which allow unused available banks to be switched around where needed; saving $$$$. This needs some programming overhead, but you have ROOM for it.

AUTO-CONFIGURATION

This is where the computer is programmed to go out to explore the neighborhood. Whatever it finds is recorded into a system configuration table (SYSCON) for later reference.

THIS IS NOT EASY!

A DUMB device cannot be found because it cannot answer a roll-call. It is deaf to attention-getting methods. It can be made visable by attaching a baby-sitter chip which can respond and identify itself and the attached device.

A SMART device listens, answers, and often calls for attention Still, it must also accept an order to shut up so it won't interrupt. The IEEE488 system is a system for standardizing command language between widely different computers and devices, but it is still not smart enough to keep quiet when another device with the same 'name' is on the system bus.

Duplicate names can be resolved if they are at different addressable locations. In this way, one of the names can be changed to avoid future confusion and wasted time. It only needs to be done initially, or when some outside event has created another duplication (Like turning on a disc drive).

A DAISY CHAIN is one way to resolve the unique address problem

Another common method is to give back-plane slots an address on a temporary basis. (Perhaps expandable using a DAISY CHAIN.)

Both methods assume something about the design of the connecting NETWORK. It must guarantee reaching only one device at a time.

NETWORKING

Almost by definition, a network is where Murphy lives. Frequently the unexpected happens. No more than three points will be made here.

1. Statistical methods must be used to find time slots when but confusion is absent by chance.
2. If this works, there is no need for physically unique addresses, though default names still help.
3. Any device connected to a network can help by introducing a random delay that is natural to the system.

BANK SWITCHING

A bank switching controller (BSC) is essentially a network switchboard. The TS2068 operating system expects eight equal 8K wide channels assigned arbitrarily to CHUNKS.

The Z80, like most CPUs, has channels to internal registers; and internally swaps between register sets. It is a bank switching controller itself.

Machine code includes extended addressing provided by additional fetched bytes. Prefix bytes allow instruction sets to be bank switched.

The 8088 CPU used in the IBM PC and clones has four dedicated internal bank switching registers whereas the Z80 has none. This idealistic approach for the 8088 worked like a charm until it ran into deep water. It outgrew it's island and couldn't build a boat Externally, bank switching registers do not have these limitations.

The BSC in Figure 1 is similar to the one inside the 8088, but there the resemblance ends. It has eight channels instead of four, and can address sixteen times as much space.

There are better BSCs than the one in Figure 1, but this one does a POWERFUL job. It also requires no alteration of your precious TS2068, a good compromise.

BANK SWITCHED OPERATION

The most significant three bits of Z80 address space are used to select one of eight previously established address extension bytes in a current chunk owner table (CCOT). The remaining bits address locations within each 8K channel.

When power is first turned on, and at other times when the TS2068 needs exclusive control, CCOT must be turned OFF. Turning it ON could be a problem.

Fortunately we can first assign all eight channels to HOME. The extended address is 255 for which nothing usually responds. Then nothing happens when CCOT is turned ON. (The 'usually' reference is explained later.)

With CCOT turned OFF extended address bits float, unless something is connected to force them high. In effect, the OFF condition also gives 255 for the extended address. That is exactly why HOME bank was assigned that bank number.

BANK SWITCHING CONTROL

Except during power-up there is no safe place in physical memory to put bank switching code. Only the fetched instruction in the Z80 is immune. That instruction must be able to find the BSC regardless of memory assignments. It must use I/O (another example of Z80 bank switching). Because GO TO and CALL are not I/O instructions, and the machine stack is unsafe anyway, each bank chunk using these needs to support them with MACROS having the same effect. The same applies to the RETurn instruction.

The most elegant method avoids using these by continuing the code in the shadowing bank and leaving the chunk with the current machine stack untouched.

This flexibility is what makes multitasking and multiuser time sharing systems remarkably easy to create. Each user can have his own private partition under control of a SUPERVISOR. Security from program interference remains a problem with the Z80, not like other CPUs which provide privileged instructions. Certain programming conventions will have to be followd to compensate for this.

There is great pressure to reserve one chunk to one bank to hold the system variables (SYSVARs), machine stack and bank switching routines. This is the technique used in the relics of machine code remaining in the unmodified TS2068. If repeated in each user's partition, this is a good convention to use. It should be remembered that it is still a convention, and need not be followed.

The relics use memory mapped bank switching ports. Unless these port addresses are forbidden to be used in all banks, it doesn't work. The BUG consists of stacking the port byte from one bank and restoring it in another, thereby destroying it in the new bank. There is a way to switch stacks to resolve this problem, but is too complex for serious considerations.

Global SYSVARs can be stored in I/O space, so this is not a real difficulty. The same applies to a bank switching stack run by the MACROS already mentioned. An alternative for the bank switching stack is to dedicate a fixed bank and chunk for it, though this has the problem of not remaining safe from accident.

MOST OF THIS DOES NOT APPLY TO THE BSC IN Figure 1. IT WAS BEEN INCLUDED TO SHOW WHAT CAN BE DONE WITH A MORE ADVANCED VERSION.

Control is simple. This BSC is write-only. It has eight ports of which only four are presently used. The port assignments avoid those to which the ZX and TS2040 printers respond and all known physical interface ports like the MODEM and TASMAN.

PORT	DATA	FUNCTION
132	x	Turn CCOT OFF
133	x	Turn CCOT ON
134	Bank #	Owner to be posted to CCOT
135	"HS"	CHUNK mask, active LOW

Bank # is identical to the extended address byte.
OUT 134, Bank # writes the bank number into a register which maintains it as input to CCOT.
"HS" is the "Horizontal Select" described by TIMEX. Looking at the structure of CCOT, it make sense.
OUT 135, HS latches the stored Bank # into CCOT registers for which HS bits are active LOW.

Some of the more signigicant bits can be ignored in smaller systems, which explains why EXROM is Bank # 254 and DOCK is Bank # 0. A system using only the lower nibble can still address one megabyte of memory.

Control can be safer from accident by using one of the unused ports to act as "SIMON SAYS". This was the real purpose of the TIMEX RESET NIBBLE SEQUENCE bank switching instruction, though never explained.

EXCEPTIONAL CONDITIONS

Bank numbers from 1 through 253 are gravy, but what about HOME (255), EXROM (254), and DOCK (0)? Can they be implemented as real external banks? The answer is definitely yes, with some limitations.

HOME ROM can be replaced with EPROM at the drop of a hat. An almost trivial case is replacing it with **SPECTRUM ROM**. What is NOT trivial is the resulting SPECTRUM having bank switching capabilities! Repairs to the TS2068 ROM code can be made in EPROM with impunity. Unlike other banks, bank 255 is active immediately at power-up. Because SPECTRUM is a subset of TS2068, it remains a toy with which to play. The real power lies in installing upward compatible extensions to BASIC and to restore TIMEX disabled functions like OPEN, CLOSE, RESET, and CATalogue.

EXROM cannot be directly replaced without removing it from the case, and even then, it is not available during power-up. The problem with internal EXROM is that it is incompletely addressed so an image of it appears in all chunks, not just chunk 0. The addressing problem can be solved by moving the chip to a special card which plugs into the cartridge slot. This card doesn't change anything except to provide full addressing to suppress the fase images. Of course, if EXROM is replaced with EPROM you can make repairs to code. In any case, you now have chunks 1 through 7 of Bank # 254 (enabled by EXROM signal) which you are free to use. On the expansion bus bank # 254 will have priority over this, but it is not active during initialization.

DOCK is usually enabled by the ROSCS signal available at the cartridge slot. If you relocate it to the expansion bus as Bank # 0, it has priority when ON, or can act the same because the ROSCS signal is available on the expansion bus.

If you have no back-plane, the EXROM relocation card is the perfect place to include replacement HOME ROM using a technique described in another article for recovering the ROMCS signal logically—as it is not available at the cartridge slot.
For the same reason, this card should carry a replacement card edge connector so you can still use your cartridges.
Should you desire, once the system has been initialized, and you DO have an expansion bus, even these replacements can be replaced by the external higher priority back-plane cards. When this is done, EXROM and DOCK are no longer mutually exclusive.

SUMMARY

While the Bank Switching System described in Figures 1 and 2 has limits on what it can do, it should start a revolution.
It is simple enough to understand, uses easily obtainable parts, and any reasonable competent hardware hacker can build it. It doesn't put your TS2068 at risk, and even if EXROM is relocated, there are no wiring changes internally so you can always put it back.
A lot of mental sweat went into creating this version. The main reason for it is to give the user confidence that it can indeed be done as advertised. Perhaps later someone will actually believe that a full self-configuring system actually exists (which it does).
It nevertheless is one **GIANT STEP** for the TS2068.

ONCE TAKEN —— WATCH OUT!

APPENDIX A

When the clock is speeded up to the point when memory boards cannot keep up, a "hold it!" signal can tell the system to give it more time until it catches up. This is called HOLD or WAIT, depending on the processer (WAIT for the Z80).
In a system where other bus masters like DMA controllers are present, and there is a good chance some of them will be too fast for the memory, the memory board must issue WAIT until it has responded properly.
Most of the time a bus master will not be kept waiting because the WAIT pulse has vanished by the time it is checked.

Referring to Figure 2, the active low BE signal can be used to trigger a one-shot flip-flop to generate a short delay pulse. Clock cycle delays cannot be used because there is no way to tell in advance how fast the clock will be running (which was the problem to begin with). The only advantage of clock cycle delays is when a known clock speed is too fast, and slow-poke memory chips are used to save money. Even in that case, the one-shot method is more efficient. Exceptions exist where memory boards contain their own clocks. Core and dynamic memory controller refresh boards belong to this category, and are intermediate in efficiency because of a random sychronization delay as well.

When polling for the presence of devices with the goal of mapping system configuration, neither the WAIT nor BE signals are of any use. In order to read bank status there must be an I/O port on each reporting device which is keyed to the bank number. The BSC drives the extended address from the selected bank number instead of CCOT. The data returned could be anything, but interrupt pending status and whether the bank is even there are both mandatory information. These bits must be active low in case nothing is there. During this read, it is the BSC which pulls up the data bus. Device status registers use open collector TTL.

Figure 1: Bank Switching

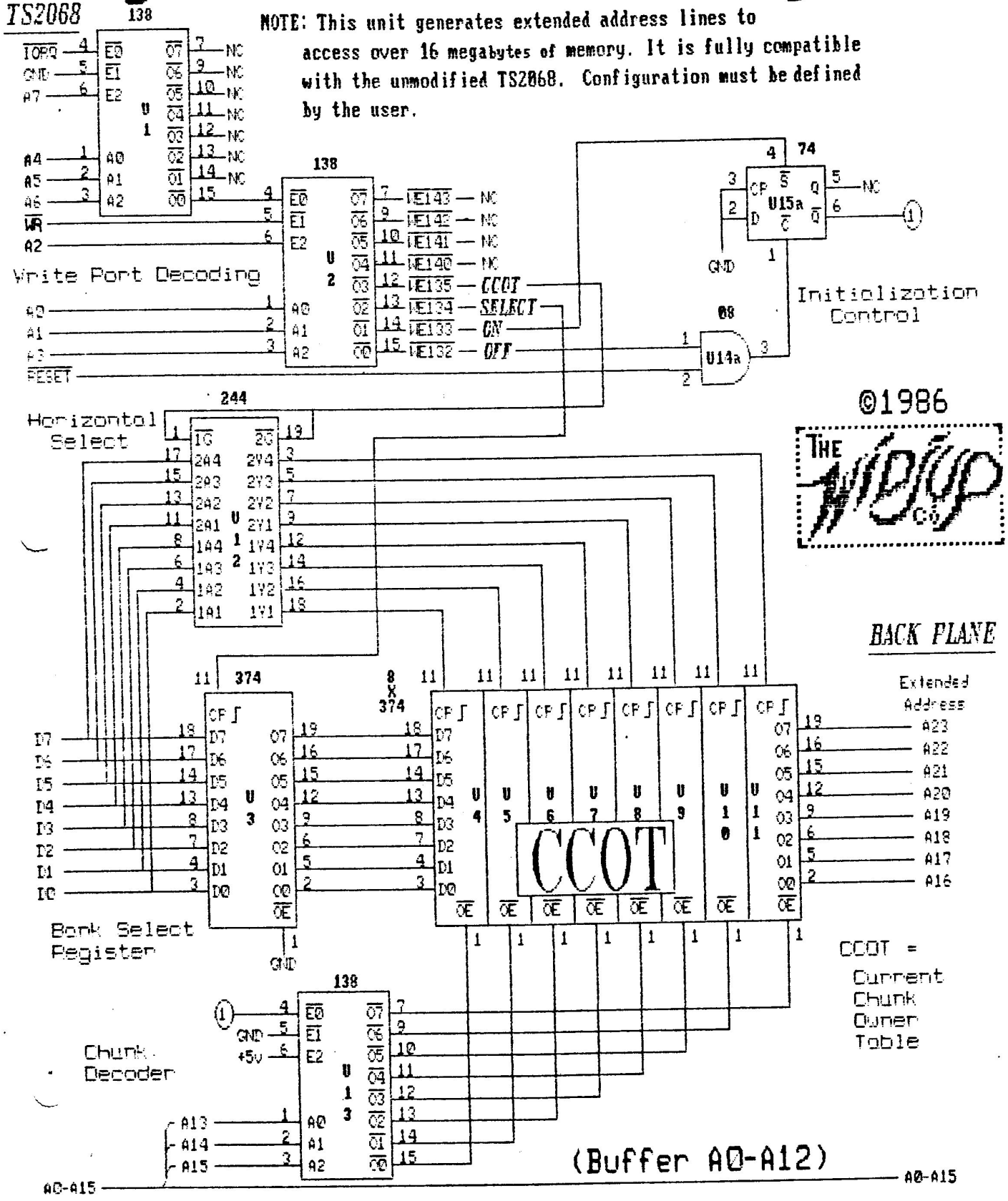
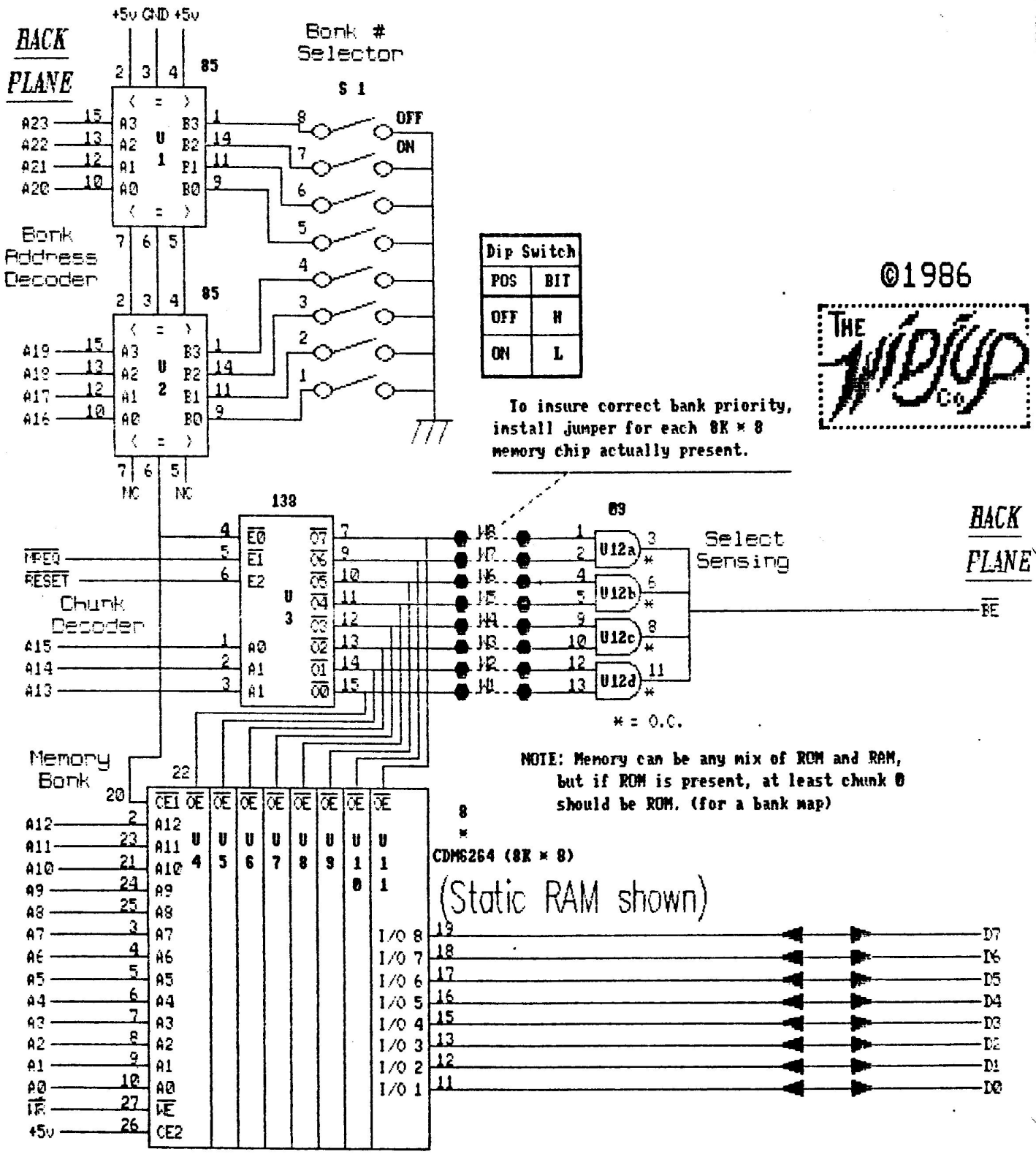


Figure 2: Memory Bank



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The TIMEXsinclair Cont.

An I/O write to a bank resets the interrupt pending register. This will also reset the INTerrupt bus signal if no other devices have interrupts pending. Interrupts issued by devices not currently owning chunks are easily found this way so their banks can be enabled to handle the interrupt. A bank number list is used to service interrupts in priority sequence. An interrupt not found in a configured bank or for the keyboard means that a new device has come on line and the auto-configure procedure must be done again.

When a DAISY CHAIN is used, the Bank # dip switches are replaced with a write-only and clear I/O port register so each card can be assigned a unique "name". This I/O port is enabled by the status of the DAISY CHAIN. A global I/O write resets both the DAISY CHAIN and the "name" registers. Bank # 0 cannot be used with a DAISY CHAIN system and special provisions are needed when HOME and EXROM are relocated anywhere but the cartridge slot or equivalent.

Once the current DAISY is named, it can be addressed directly to read status, and written to if applicable. When a nonexistent Daisy is given a name and then asked for status, there is no answer of course. This signals the end of the CHAIN.

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